Sign in

Google

Web Images Video News Maps more »

load store register overflow spill instruction pai Search Advanced Search Preferences

Web Results **1 - 10** of about **34,300** for **load store register overflow spill instruction parallel complex archi**

Pairing of spills for **parallel** registers - Patent 20050005267
A method of handling **register** spills in a **parallel register architecture**, ... **Parallel** intermediate **load/store spill instructions** are rewritten as actual ...
www.freepatentsonline.com/20050005267.html - 44k - Cached - Similar pages

Great Microprocessors of the Past and Present: Born Beyond Scalar
Like many other **load-store** CPUs, **register** R0 is treated as constant 0 for ... but it allows multimedia **instructions** to be executed in **parallel** with both ...
www.microprocessor.sscc.ru/great/s5.html - 25k - Cached - Similar pages

[PDF] Inter-Procedural Stacked RegisterAllocation for Itanium Like ...
File Format: PDF/Adobe Acrobat - View as HTML
register assignment could save 50 cycles (100x0.5 = 50) by. eliminating the corresponding explicit **load/store spill**. **instructions**, but it incurs 100 cycles ...
ipf-orc.sourceforge.net/ICS-184.pdf - Similar pages

[PDF] DSP : A C -B C D S P
File Format: PDF/Adobe Acrobat
Harvard **load-store architecture**. Figure 1 gives ... of a SIMD **instruction** in **parallel**. The structure of the **register** file is orthogo- ...
ieeexplore.ieee.org/iel5/40/29395/01331280.pdf?arnumber=1331280 - Similar pages

[PDF] S P C ' M A
File Format: PDF/Adobe Acrobat
The SPU **architecture** is based on perva-. sively data **parallel** computing (PDPC), ... formatting and. permute unit. **Load/store**. unit. 2 **instructions**. 64 bytes ...
ieeexplore.ieee.org/iel5/40/34097/01624323.pdf - Similar pages

Synergistic Processing in Cell's Multicore **Architecture**
The SPU **architecture** implements a novel, pervasively data-**parallel** ... It **stores instructions** in **instruction** line buffers and delivers them to the execution ...
doi.ieeecomputersociety.org/10.1109/MM.2006.41 - Similar pages

[PDF] LLVA: A Low-level Virtual **Instruction** Set **Architecture**
File Format: PDF/Adobe Acrobat - View as HTML
The **instruction** set is typed,. uses an infinite virtual **register** set in Static Single Assign- ... tore **architecture**: only **load** and **store instructions** ac- ...
www.microarch.org/micro36/html/pdf/adve-LowLevelVirtual.pdf - Similar pages

[PDF] Understanding the IA-64 **Architecture**
File Format: PDF/Adobe Acrobat - View as HTML
use =r1. Traditional Architectures. Barrier. **Load** moved. above **store**. by compiler ... IA-64 FP **register** resources enable sufficient **parallel** ...
www.csee.umbc.edu/help/**architecture**/idfisa.pdf - Similar pages

[PDF] **Register** Pointer **Architecture** for Efficient Embedded Processors
File Format: PDF/Adobe Acrobat - View as HTML
The **Register** Pointer **Architecture** (RPA) supports large. **register** files to reduce the time and ... formance gain from the **load** and **store instruction** elimina- ...
csl.stanford.edu/~christos/publications/2007.rpa.date.pdf - Similar pages

Sign in

Google

Web Images Video News Maps more »

reuse register overflow spill fill instruction para Search Advanced Search Preferences

Web Results **1 - 10** of about **17,800** for **reuse register overflow spill fill instruction parallel complex archite**

Itanium Processor Microarchitecture
The processor employs EPIC (explicitly **parallel instruction** computing) design ... of NaT bits and NaTVals also affect the **register spill**-and-**fill** logic. ...
doi.ieeecomputersociety.org/10.1109/40.877948 - Similar pages

[PDF] Design and Applications of a Virtual Context **Architecture**
File Format: PDF/Adobe Acrobat - View as HTML
would be the size of the **instructions**. As stated previously a **register** ... a **spill** or **fill** is necessary. On the other end, the ASTQ feeds a mux that merges ...
www.eecs.umich.edu/techreports/cse/2004/CSE-TR-497-04.pdf - Similar pages

[PDF] Itanium processor microarchitecture - Micro, IEEE
File Format: PDF/Adobe Acrobat
affect the **register spill**-and-**fill** logic. For. explicit software-driven **register** spills and fills,. special move **instructions** (store.**spill** and ...
ieeexplore.ieee.org/iel5/40/18997/00877948.pdf?tp=&arnumber=877948&isnumber=18997 - Similar pages

[PDF] MAQAO: Modular Assembler Quality Analyzer and Optimizer for Itanium 2
File Format: PDF/Adobe Acrobat - View as HTML
In that more **complex**. case, the **fill** and **spill instructions** corresponding to r44 can be removed. Dynamic Analysis Replacing theses **instructions** with nops or ...
www.prism.uvsq.fr/~bad/Research/ps/maqao.pdf - Similar pages

Task flow computer **architecture** - Patent 5574933
Transmission packets communicate **instructions** and **register** values along the linked list. ... it may be advantageous to **spill** the **overflow** TPs into memory. ...
www.freepatentsonline.com/5574933.html - 71k - Cached - Similar pages

Diamond Standard Processor Core Family **Architecture**
The Diamond processors delay window **overflow** until absolutely necessary, creating fewer **register-spill** traps and smaller code size compared to other ...
www.us.design-**reuse**.com/articles/article14621.html - 104k - Cached - Similar pages

[PS] Compiler Optimization to exploit Pipeline registers and Forwarding ...
File Format: Adobe PostScript - View as Text
register reuse. To minimize these dependencies, pre-pass code scheduling moves **instructions** closer to. their potential **fill** slots, thus increasing the live ...
www.cse.iitd.ernet.in/esproject/homepage/docs/projects/2003-2004/bypass_opt_mtp_final.ps.gz - Similar pages

Task flow computer **architecture** - US Patent 5574933
Current approaches to **parallel** processing include Single **Instruction** Multiple Data (SIMD) ... it may be advantageous to **spill** the **overflow** TPs into memory. ...
www.patentstorm.us/patents/5574933-description.html - 64k - Cached - Similar pages

[PDF] Intel Itanium 2 Processor
File Format: PDF/Adobe Acrobat - View as HTML
With longer and more **complex instruction** streams,. With longer and more **complex instruction** streams ... Avoid **Register Spill/Fill** Upon Procedure Call/Return ...